

AMENDMENT TO THE SPECIFICATION

Replace the existing abstract in its entirety with the following abstract:

-- A method utilizing available timing slack in the various timing paths of a synchronous integrated circuit to reduce the overall instantaneous current draw across the circuit. In the method, each timing path is analyzed to determine its late mode margin or its late mode margin and early mode margin. A delay is added to each timing path having a late mode margin greater than zero. Each delay effectively shifts the peak current draw for the corresponding timing path within each clock cycle so that the peaks do not occur simultaneously across all timing paths. In other embodiments, the peak overall instantaneous current draw can be further reduced by reducing the delay in some of the delayed timing paths.--